REMARKS

The rejections of Claims 12-14 under 35 USC §112, ¶¶s 1 and 2, are traversed. Reconsideration of those rejections is requested based upon the above amendments and following comments.

The reference to Claim 15 in the first paragraph on page 3 of the Office Action is not understood in light of the Examiner's conclusions found in the second paragraph on page 2 of the Office Action. Applicants inquire as to whether the Examiner is acting on the merits of Claims 15 and 16.

Applicants have specifically addressed the antecedent issue with regard to "said integrated circuits" by amending the term in Claim 12 to be singular.

The terms now used in the claims have clear antecedent bases and full support in the written description. For example, reference to the voltage source circuit for outputting electrical power begins at paragraph [0011] of the Substitute (and original) Specification as does the term "integrated circuit" to which there are also numerous references in the written description as well as reference to integrated "circuits" [0013] and an integrated circuit arithmetic processing unit [0019]. One of ordinary skill in the art will have no reason to question either the adequacy of the written description to support the claim terms or the reasonable manner in which the Applicants have defined the metes and bounds of their invention.

The rejection of Claims 12 and 14 as being anticipated by Ovens et al under 35 USC §102(b) and the rejection of Claim 13 as being unpatentable over Ovens et al under 35 USC §103(a) are traversed. Reconsideration of these rejections is requested on the following grounds.

The Ovens et al test circuit 10 shown in Fig. 1 is separately provided in a wafer near a semiconductor circuit to be tested. The NODE 1 is supplied a higher voltage than a breakdown voltage of a Zener diode 12 to enable the test circuit 10 and is connected with the actual semiconductor circuit during a test mode so as to add the higher voltage to the actual semiconductor circuit. Here, as an electric current flows through the NODE 1, the terminal voltages of resistors 26, 34 are detected as are the betas of the NPN transistors, whereby any discrepancy from design values of the resistors in the actual circuit can be estimated.

Therefore, the test circuit 10 is not always connected to the actual circuit in order to supply a rated voltage to the actual circuit. This connection only occurs when the test circuit 10 is enabled by taking V_{CC} to zero volts (ground) and applying a voltage above the Zener breakdown voltage to NODE 1.

In the claimed present invention, the voltage source circuitry 100 is always connected to a tested circuit, i.e., integrated circuit 111, 112, 113, through the output side power line 110 so as to supply the rated voltage to the actual circuit. In such a circuit, when a switch 105, 204 is ON in the test mode, a higher voltage than the reference voltage is fed to said integrated circuit 111, 112, 113 through the output side power line 110.

In light of the foregoing, it should also be clear that Ovens et al does not teach a switch as claimed in this application and certainly does not suggest an arrangement in which a mechanical switch could be employed in the claimed manner. The asserted "switch" 36 of Ovens et al is an NPN transistor and is not functional to feed the claimed higher voltage to the integrated circuit for

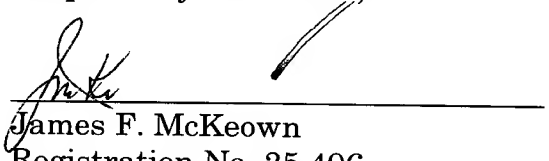
performing the screening operation. The allegation of substituting a mechanical switch is without any basis or suggestion in Ovens et al and is purely speculative. Impermissible hindsight motivation is the real prime mover for the alleged substitution. The Office Action does not set forth a prima facie case of obviousness based on objective and substantial record evidence.

Therefore, one of the objects of the present invention in feeding both the normal rated voltage and the higher voltage during the test mode through the same output side power line 110 is not taught or suggested in Ovens et al.

Accordingly, reconsideration of the rejections and favorable action on the claims are earnestly solicited.

If necessary to effect a timely response, this paper should be considered as a petition for an Extension of Time sufficient to effect a timely response, and please charge any deficiency in fees or credit any overpayments to Deposit Account No. 05-1323 (Docket #381NP/49131).

Respectfully submitted,



James F. McKeown
Registration No. 25,406

CROWELL & MORING, LLP
Intellectual Property Group
P.O. Box 14300
Washington, DC 20044-4300
Telephone No.: (202) 624-2500
Facsimile No.: (202) 628-8844
JFM:kms 56207